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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,123	07/30/2001	Subhash C. Roy	TRA-040 C1	1388

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EXAMINER	
WHITMORE, STACY	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,123	ROY ET AL.	
	Examiner	Art Unit	
	Stacy A Whitmore	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/3/2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 19-35 are presented for examination.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 19-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Hervin (US Patent 6,205,560).

4. As for claim 19, Hervin disclosed the invention as claimed, including a method of debugging a processor, said method comprising:

providing information about processor activity in real time [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-555; col. 12, line 64- col. 13, line 2];

associating the instructions executed by the processor with information about processor activity [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-555; col. 12, line 64- col. 13, line 2], wherein said providing information about processor activity includes providing information about substantially every instruction executed by the processor including instructions other than breakpoint instructions [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-55; col. 12, line 64- col. 13, line 2 and 50-55].

5. As for claim 25, Hervin disclosed the invention as claimed, including a method of debugging a processor, said method comprising:

providing information about processor activity in real time according to a first clock [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-555; col. 12, line 64- col. 13, line 2]; and

associating the instructions executed by the processor with the information about processor activity according to a second clock [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-555; col. 12, line 64- col. 13, line 2].

6. As for claim 31, Hervin disclosed a method of debugging a processor, said method comprising:

causing the processor to provide information about processor activity in real time [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-555; col. 12, line 64- col. 13, line 2]; and

causing a debugger to associate the instructions executed by the processor with the information about processor activity [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-55; col. 12, line 64- col. 13, line 2].

7. As for claim 26, Hervin disclosed the first clock is the processor clock and the second clock is a debugger clock [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-55; col. 12, line 64- col. 13, line 2: the TCK is the second clock].

8. As for claims 23, 24, 27, and 35, Hervin further disclosed wherein said providing information is performed by the processor, and said associating the instructions is performed by debugger [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-555; col. 12, line 64- col. 13, line 2: especially lines 45-47 of col. 12, where Hervin discloses that the JTAG routine which controls the recording of state data and the processor that executes the program is providing the information]; and wherein said step of providing information about processor activity in real time is performed according to a first clock; and said step of associating the instructions executed by the processor with the information about processor activity is performed according to a second clock [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-55; col. 12, line 64- col. 13, line 2: the second clock is the TCK].

9. As for claims 20, 28, and 32, Hervin disclosed the providing information about processor activity includes providing an indication every time the processor stalls that the processor has stalled [col. 16, line 5 – col. 7, line 5; col. 16, lines 35-60].

10. As for claims, 21, 22, 29-30, and 33-34, Hervin disclosed the information about processor activity includes information as to at least one of whether the last instruction executed was a jump, a jump based on contents of a register, a branch taken, or an instruction which encountered an exception [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-555; col. 12, line 64- col. 13, line 2; col. 9, Table 3], and providing information regarding the status of the processor when certain processor events occur, said certain processor events including at least one of a change in status of an interrupt line, an internal processor exception, and the execution of a jump based on the contents of a register [col. 2, lines 1-9, and 30-51; col. 12, lines 20-30 45-555; col. 12, line 64- col. 13, line 2; col. 9, Table 3].

11. Claims 19, 21-22, 25, 29-31, and 34-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Deano (US Patent 6,081,885).

12. As for claim 19, Deano disclosed the invention as claimed, including a method of debugging a processor, said method comprising:

providing information about processor activity in real time [col. 57, lines 15-30];

associating the instructions executed by the processor with information about processor activity [col. 57, lines 15-30, the result of the debug is the association of instructions with information about processor activity], wherein said providing information about processor activity includes providing information about substantially every instruction executed by the processor including instructions other than breakpoint instructions [col. 57, lines 15-30, this includes instructions other than breakpoint instructions because the debugging occurs in real time with substantially every instruction which inherently include instructions other than breakpoint instructions].

13. As for claims 21, 22, 29-30, and 33-34, Deano disclosed the invention as claimed, including the information about processor activity includes information as to at least one of whether the last instruction executed was a jump, a jump based on contents of a register, a branch taken, or an instruction which encountered an exception

[col. 27-28], and providing information regarding the status of the processor when certain processor events occur, said certain processor events including at least one of a change in status of an interrupt line, an internal processor exception, and the execution of a jump based on the contents of a register [col.27-28].

14. As for claim 25, Deano disclosed the invention as claimed, including a method of debugging a processor, said method comprising:

providing information about processor activity in real time according to a first clock [col. 57, lines 15-30]; and

associating the instructions executed by the processor with the information about processor activity according to a second clock [col. 57, lines 15-30, the result of the debug is the association of instructions with information about processor activity; col. 59, lines 59-67].

15. As for claim 31, Deano disclosed a method of debugging a processor, said method comprising:

causing the processor to provide information about processor activity in real time [col. 57, lines 15-30]; and

causing a debugger to associate the instructions executed by the processor with the information about processor activity [col. 57, lines 15-30].

16. Claims 20, 28, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deano (US Patent 6,081,885) in view of Segars et al. (6,052,774).

17. As for claims 20, 28, and 32, Deano disclosed the invention substantially as claimed, including the method of debugging a processor as cited in the rejections of claims 19 and 31 above.

Deano did not specifically disclose providing information about processor activity includes providing an indication every time the processor stalls that the processor has stalled.

Segars disclosed providing information about processor activity includes providing an indication every time the processor stalls that the processor has stalled [col. 13, especially lines 48-67].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Deano and Segars because providing information every time the processor stalls would allow for Deano's method to improve the debug function by only providing debug information when the processor is active, which would improve Madduri's debug system by requiring no output when it is not needed for debug information.

18. Applicant's arguments filed 11/3/03 have been fully considered but they are not persuasive and are moot in view of new grounds of rejection.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Stacy A Whitmore
Primary Examiner
Art Unit 2812

SAW
January 9, 2004